REMARKS

The Office Action dated February 25, 2004, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

As a preliminary matter, Applicants appreciate the indication of allowable subject matter in claims 2, 4, 7, and 8 of the present application.

Claims 6 has been amended, and claim 9 has been cancelled without prejudice. Applicants submit that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1-8 are pending in the present application and are respectfully submitted for consideration.

The title of the invention was not descriptive. Applicants respectfully submit a more descriptive new title of -- **SEMICONDUCTOR MEMORY DEVICE CAPABLE OF SIMULTANEOUSLY READING DATA AND REFRESHING DATA** --.

Claims 1, 3, 5, 6, and 9 were rejected under the judicially created doctrine of double patenting over claims 1 of U.S. Patent No. 6,421,292 to Kitamoto et al. (hereinafter "Kitamoto") in view of claim 1 of U.S. Patent No. 6,529,435 to Yagishita et al. (hereinafter "Yagishita"). In making this rejection, the Examiner took the position that, although the claims of the present invention and the claims of the Kitamoto patent in view of the Yagishita patent are not identical, they are nevertheless, not patentably distinct from each other since Kitamoto in view of Yagishita teach all the necessary structural features to enable one of ordinary skill in the art to conclude that claims 1, 3,

5, 6 and 9 of the present application recite obvious variations of the claims of Kitamoto in view of Yagishita.

Claim 9 has been canceled and therefore the rejection is now moot.

Applicants respectfully traverse the double-patenting rejection and submit that the claims recited in the present invention defines an invention that is **not** merely an obvious variation of Kitamoto in view of Yagishita.

Claim 1 recites a semiconductor memory device capable of simultaneously reading data and refreshing data. The semiconductor memory device comprises a data inputting circuit for receiving data inputted from an external circuit, a parity generating circuit for generating parity data from the data input from the data inputting circuit, and a memory for storing the data input from the data inputting circuit and the parity data generated by the parity generating circuit. In addition, the semiconductor memory device includes a refreshing circuit for refreshing the memory, a reading circuit for reading the data from the memory, a restoring circuit for restoring data to be refreshed by the refreshing circuit from other data read normally and corresponding parity data, while the reading circuit is reading data, a data outputting circuit for outputting the data read by the reading circuit and the data restored by the restoring circuit, and a parity outputting circuit for directly reading and outputting the parity data stored in the memory.

Claim 3 recites a semiconductor memory device capable of simultaneously reading data and refreshing data. The semiconductor memory comprises a data inputting circuit for receiving data inputted from an external circuit, a parity generating circuit for generating parity data from the data input from the data inputting circuit, and a

memory for storing the data input from the data inputting circuit and the parity data generated by the parity generating circuit. Furthermore, the semiconductor memory includes a refreshing circuit for refreshing the memory, a reading circuit for reading the data from the memory, a restoring circuit for restoring data to be refreshed by the refreshing circuit from other data read normally and corresponding parity data, while the reading circuit is reading data, a data outputting circuit for outputting the data read by the reading circuit and the data restored by the restoring circuit, and a writing circuit for directly writing desired data supplied from an external circuit in an area of the memory where the parity data is stored.

Claim 6 recites substantially parallel language as that of claim 1 with the exception of that claim 6 recites a semiconductor memory device also having a control circuit for controlling the refreshing circuit to refresh a given area according to a request from an external circuit, and a writing circuit for directly writing desired data supplied from an external circuit in an area of the memory where the parity data is stored, and the control circuit controls the refreshing circuit to refresh an area specified by the external circuit.

Claim 1 of Kitamoto recites:

> A semiconductor memory comprising:
>
> a parity generating unit which generates a first parity in accordance with a plurality of bits of write data;
>
> a memory cell array having a plurality of blocks which are simultaneously subjected to a data write or read operation, each block being provided with a plurality of sub-arrays storing the write data and one or more arrays storing the first

parity, each of the plurality of sub-arrays being provided with a plurality of memory cells;
a refresh unit which performs a refresh operation to each of the sub-arrays; and

a parity-data comparing unit which compares the first party with a second parity generated by assuming that read data from at least one of the plurality of sub-arrays which cannot be accessed because at least one of the plurality of other blocks is activated by the refresh operation when the refresh operation and the data read operation are performed at the same time is 0 or 1, to determine the write data stored in the at least one of the plurality of sub-arrays.

Claim 1 of Yagishita recites,

A semiconductor memory device in which subblocks each constituted by one or two or more memory cells are arranged in matrix form, comprising:

an address input circuit for receiving an input address;

a readout circuit for reading out data from at least part of a subblock group arranged in a column or row direction and specified by the address input via said address input circuit; and

a refresh circuit for refreshing at least part of a subblock group arranged in a row or column direction and intersecting with the subblock group from which data is read out by said readout circuit;

wherein the subblock group from which data is read out by said readout circuit includes a subblock storing parity data for restoring data, and

said semiconductor memory device further comprises a data restoration circuit for restoring data of a subblock where the subblock group from which data is read out by said readout circuit intersects with the subblock group which is refreshed by said refresh circuit, based on the parity data and data of other subblocks.

It is submit that claims 1, 3, 5 and 6 as recited in the present invention defines an invention that is **not** merely an obvious variation of claim 1 of Kitamoto in view of claim 1 of Yagishita. Specifically, claims 1, 3 and 6 recites at least the limitations of "a parity outputting circuit for directly reading and outputting the parity data stored in said memory," "a writing circuit for directly writing desired data supplied from an external circuit in an area of said memory where said parity data is stored," and "a writing circuit for directly writing desired data supplied from an external circuit in an area of said memory where said parity data is stored, and said control circuit controls said refreshing circuit to refresh an area specified by the external circuit," respectively.

However, neither claim 1 of Kitamoto nor claim 1 of Yagishita recite at least the foregoing claimed limitations of the "a parity outputting circuit," and "a writing circuit," and therefore the claims of the present invention and the claims of the Kitamoto patent in view of the Yagishita patent are not identical. More importantly, the claims of the present invention and the claims of the Kitamoto patent in view of the Yagishita patent are indeed patentably distinct from each other since Kitamoto in view of Yagishita fails to teach all the necessary structural features to enable one of ordinary skill in the art to conclude that claims 1, 3, 5 and 6 of the present application recite obvious variations of the claims of Kitamoto in view of Yagishita.

In view of the above, Applicants respectfully submit that each of claims 1, 3, 5 and 6 recites subject matter that is neither disclosed nor suggested in the cited prior art, and recites subject matter that is patentably distinct from the claims of the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the

claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1-8 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, referencing Attorney Docket No. 107337-00006.

Respectfully submitted,

Sam Huang
Registration No. 48,430

Customer No. 004372
ARENT FOX, PLLC
1050 Connecticut Avenue, N.W., Suite 400
Washington, D.C. 20036-5339
Tel: (202) 857-6000
Fax: (202) 638-4810

SH:grs

Enclosure: Petition for Extension of Time (1 month)